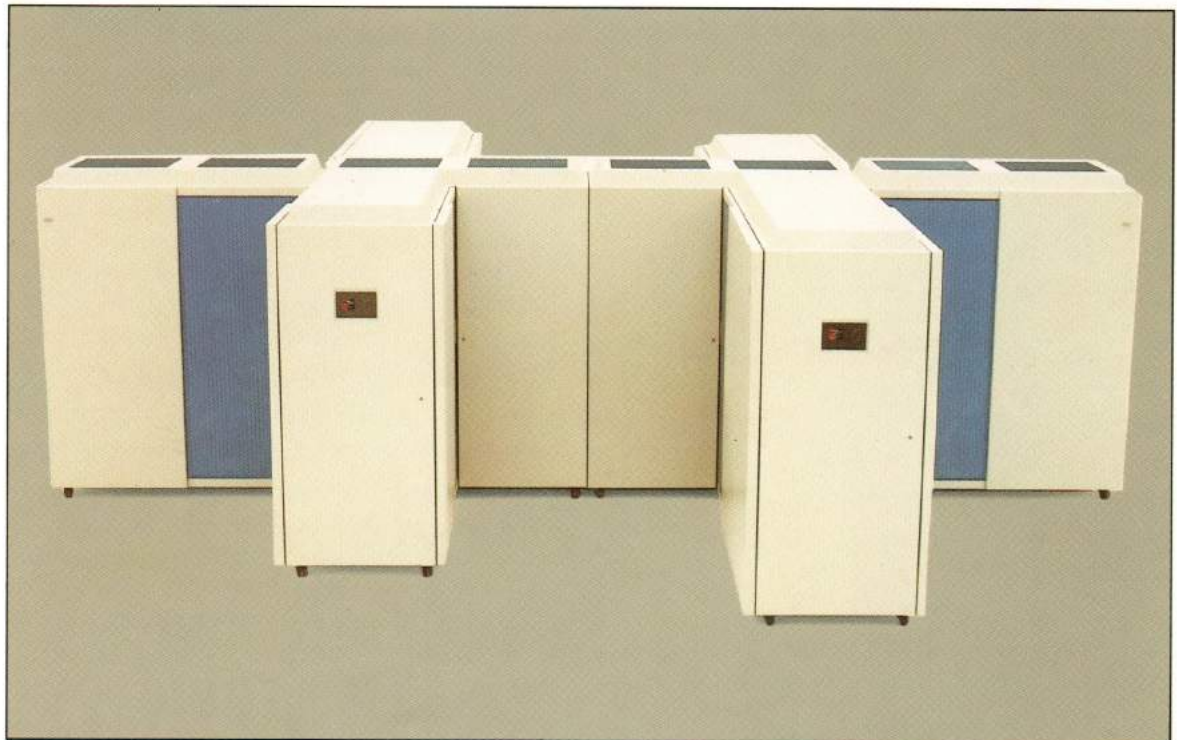
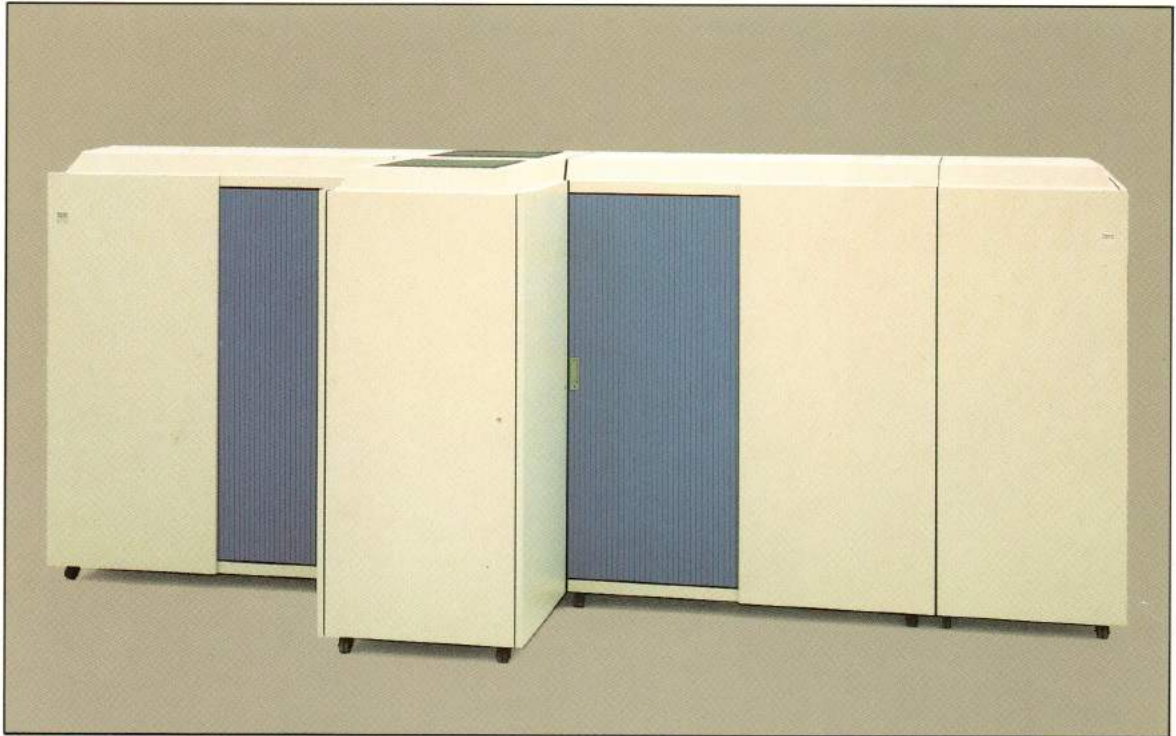
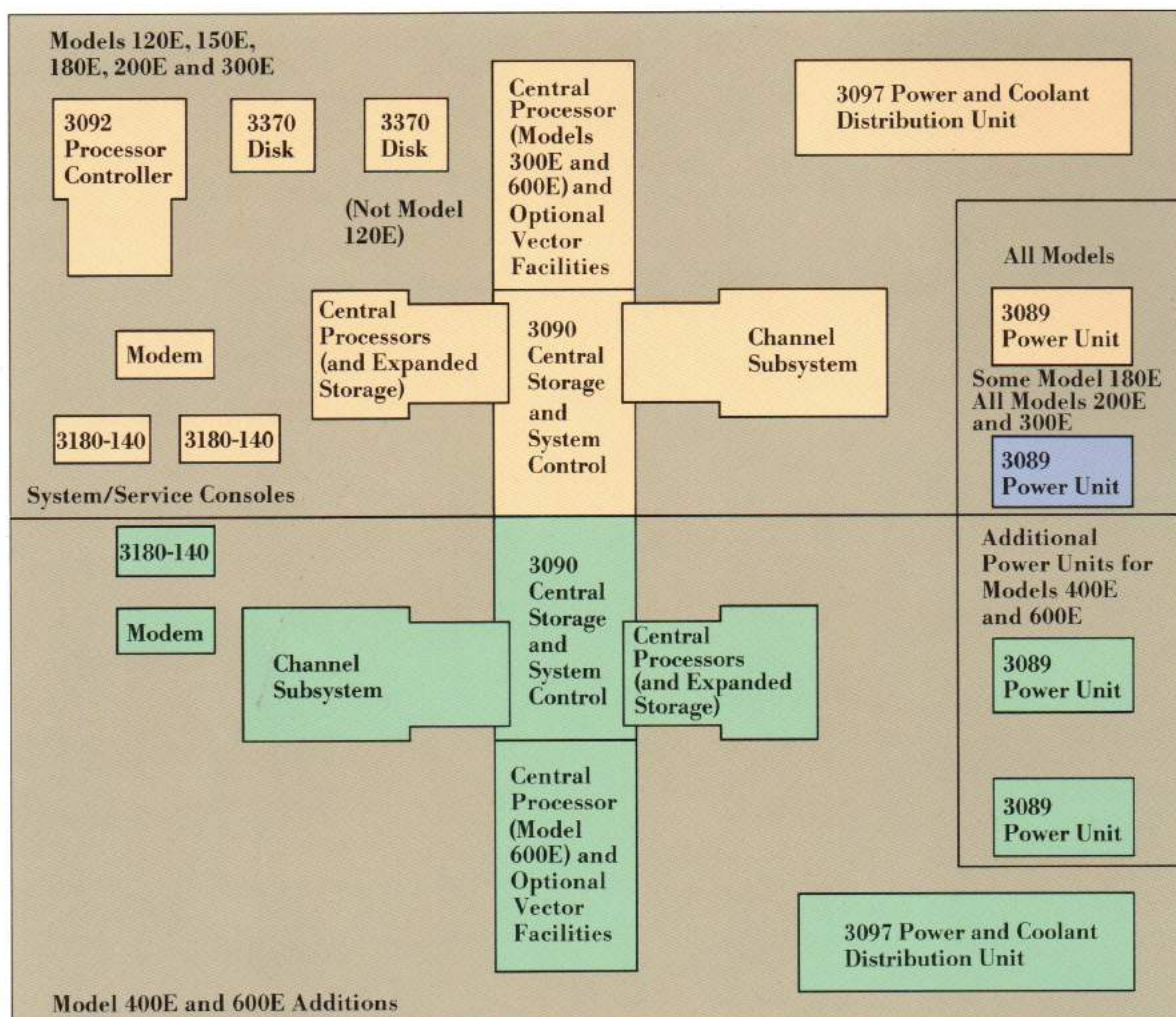


**IBM 3090
Processor Unit Models
120E, 150E, 180E, 200E, 300E, 400E and 600E**



IBM

Denne side er lagt ind for at man kan læse de følgende med tegning og tekst overfor hinanden



Enhanced IBM 3090 Processor Complex

Processor Complex Configuration

The IBM 3090 is a field-upgradeable family which consists of seven models: three uniprocessors, one dyadic, one triadic, one four-way and one six-way multiprocessor. They provide up to ten-fold growth from the smallest Model 120E to the largest Model 600E.

In addition, from one to six optional Vector Facilities (one per central processor) may be configured to provide enhanced performance and modular growth for vectorisable applications.

An IBM 3090 can be installed in approximately 11 to 17 hours. Field upgrades can be made to the next higher model in nine to 24 hours depending on the model.

All IBM 3090 Processor Complexes include:

- Two 3370 Model A2 Direct Access Storage Devices (except Model 120E, which requires one 3370 Model A2 Direct Access Storage Device).
- Two 3180 Model 140 Display Stations as system and service support consoles.
- One 3864 Model 2 Modem or a 4800 bits per second (bps) switched network modem supporting an autocall/autoanswer feature.
- One 3097 Model 1 or Model 2 Power and Coolant Distribution Unit.

An IBM 3090 Model 120E, 150E or 180E Complex, in addition to the common support units listed above, comprises:

- One 3090 Uniprocessor Processor Unit with one central processor and one optional Vector Facility.
- One or two 3089 Model 3 Power Units or equivalent 400 Hz power source. The second 3089 is only required if 192/256 Mb Expanded Storage and a Vector Facility are configured.
- One 3092 Model 1 Processor Controller (or one 3092 Model 3 for a 3090 Model 120E).

An IBM 3090 Model 200E or 300E Complex, in addition to the common support units listed above, comprises:

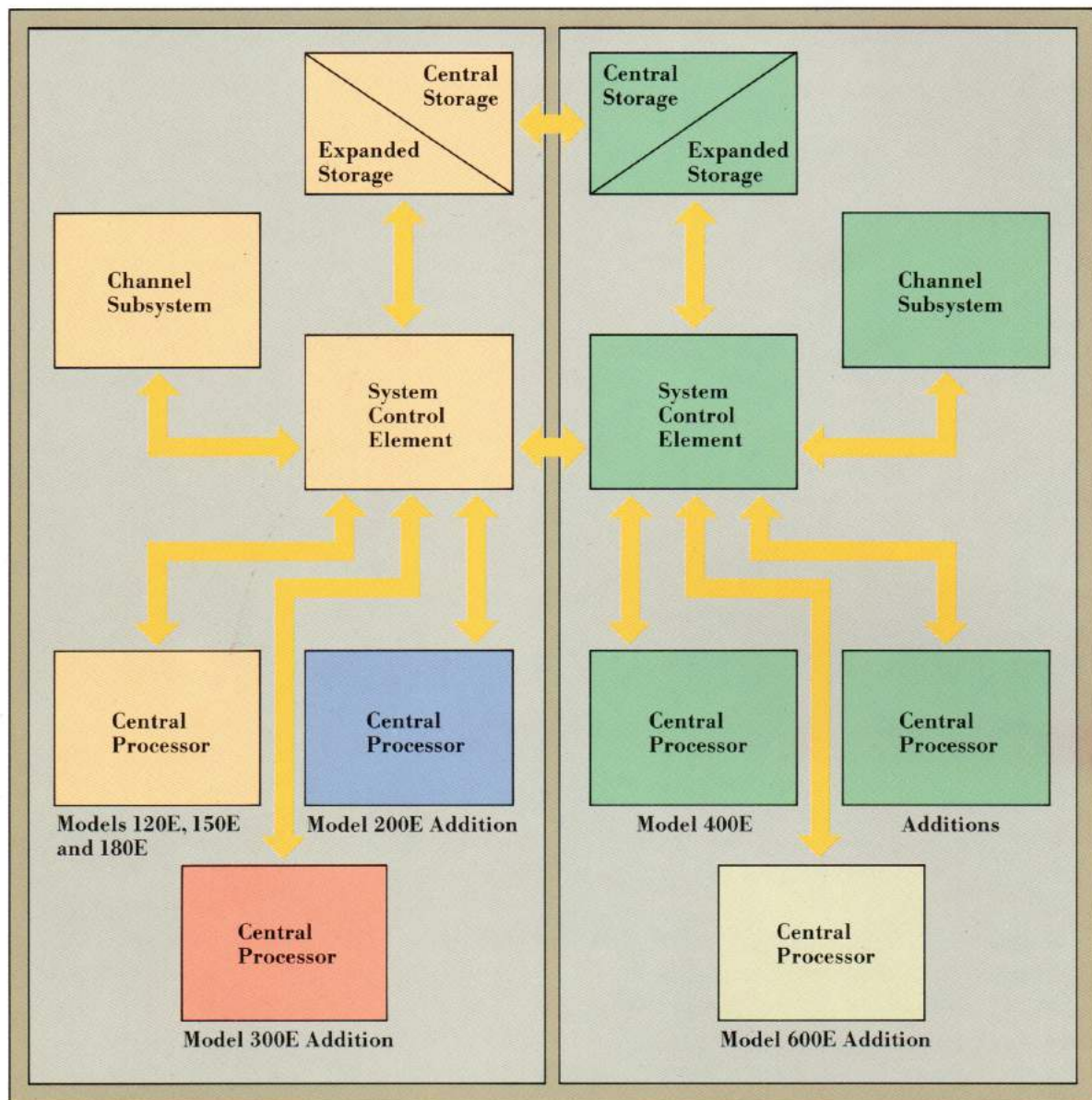
- One 3090 Model 200E Processor Unit with two central processors and one or two optional Vector Facilities, or one 3090 Model 300E Processor Unit with three central processors and one, two or three optional Vector Facilities.
- Two 3089 Model 3 Power Units or equivalent 400 Hz power source.
- One 3092 Model 1 Processor Controller.

An IBM 3090 Model 400E or 600E Complex comprises:

- One 3090 Model 400E Processor Unit with four central processors and up to four optional Vector Facilities, or one 3090 Model 600E Processor Unit with six central processors and up to six optional Vector Facilities.
- Three 3180 Model 140 Display Stations as system and service support consoles.
- Two 3864 Model 2 Modems or two 4800 bps switched network modems supporting an autocall/autoanswer feature.
- Two 3097 Power and Coolant Distribution Units. Model 1s and Model 2s may be used in any combination.
- Four 3089 Model 3 Power Units or equivalent 400 Hz power source.
- One 3092 Model 2 Processor Controller.

IBM 3090 Processor Complex Support Units and Vector Facility:

- For details on the IBM 3089, IBM 3092, IBM 3097 and other IBM 3090 Processor Complex Support Units, see the associated publication G511-0134.
- For additional details on the IBM 3090 Vector Facility and its System Software, see the associated publication G511-0136.



Enhanced IBM 3090 Processor Unit Design

Processor Unit Design

The Processor Units of the IBM 3090 family perform the data processing functions of the IBM 3090 Processor Complex and are the most powerful computers available from IBM.

All IBM 3090 Processor Units are composed of four main elements:

- Central Processor.
- System Control Element.
- Central and optional Expanded Storage.
- Channel Subsystem.

The Model 120E, a new entry-level uniprocessor, has:

- One Central Processor with 18.5 ns cycle time and one optional Vector Facility.
- One System Control Element.
- Processor Storage consisting of 32 Mb of Central Storage and 64 or 128 Mb of optional Expanded Storage.
- One Channel Subsystem with 16 or 24 channels.

The Model 150E, a uniprocessor, has:

- One Central Processor with 17.75 ns cycle time and one optional Vector Facility.
- One System Control Element.
- Processor Storage consisting of 32 or 64 Mb of Central Storage and 64 or 128 Mb of optional Expanded Storage.
- One Channel Subsystem with 16 or 24 channels.

The Model 180E, a more powerful uniprocessor, has:

- Central Processor with 17.2 ns cycle time and one optional Vector Facility.
- One System Control Element.
- Processor Storage consisting of 32 or 64 Mb of Central Storage and 64, 128, 192 or 256 Mb of optional Expanded Storage.
- One Channel Subsystem with 16, 24 or 32 channels.

The Model 200E, a dyadic processor, has:

- Two Central Processors with 17.2 ns cycle time and one or two optional Vector Facilities.
- One System Control Element.
- Processor Storage consisting of 64 or 128 Mb of Central Storage and 64, 128, 192, 256 or 512 Mb of optional Expanded Storage.
- One Channel Subsystem with 32, 40, 48 or 64 channels.
- It operates as a single logical system.

The Model 300E, a triadic processor, has:

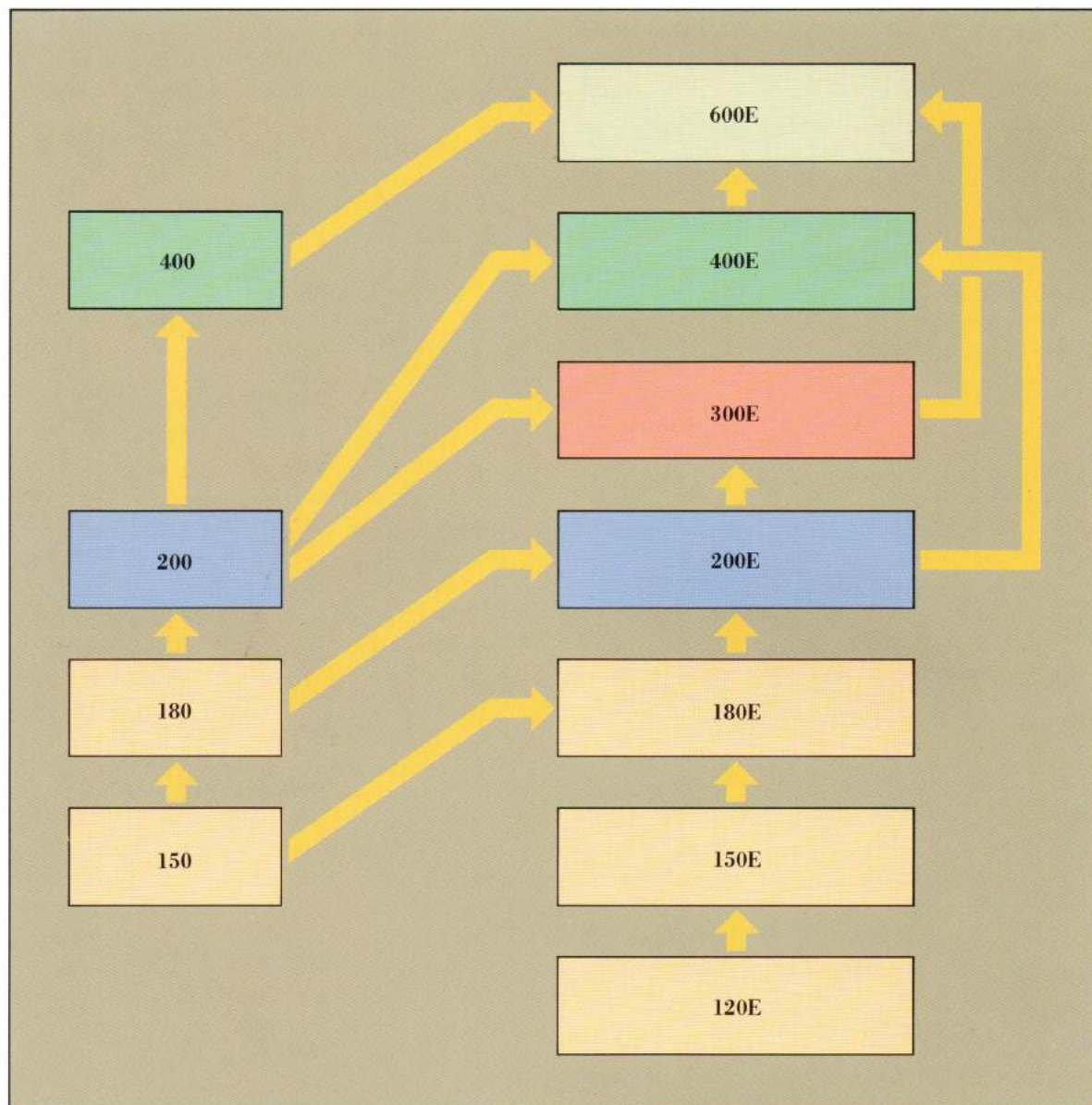
- Three Central Processors with 17.2 ns cycle time and up to three optional Vector Facilities.
- One System Control Element.
- Processor Storage consisting of 64 or 128 Mb of Central Storage and 64, 128, 192, 256 or 512 Mb of optional Expanded Storage.
- One Channel Subsystem with 32, 40, 48 or 64 Channels.
- It operates as a single logical system.

The Model 400E, a four-way processor, has:

- Four Central Processors with 17.2 ns cycle time and up to four optional Vector Facilities.
- Two linked System Control Elements.
- Processor Storage containing a total of 128 or 256 Mb of Central Storage and 128, 256, 384, 512 or 1024 Mb of optional Expanded Storage.
- Two Channel Subsystems with a total of 64, 80, 96 or 128 channels.
- It is divided into an A and a B side, each of which contains two Central Processors and one of each of the other elements, and can operate:
 - Either as a single logical system, with the A and B sides combined, in single image mode.
 - Or as two logical dyadic systems, with the A and B sides working independently, in partitioned mode.

The Model 600E, a six-way processor, has:

- Six Central Processors with 17.2 ns cycle time and up to six optional Vector Facilities.
- Two linked System Control Elements.
- Processor Storage containing a total of 128 or 256 Mb of Central Storage and 128, 256, 384, 512 or 1024 Mb of optional Expanded Storage.
- Two Channel Subsystems with a total of 64, 80, 96 or 128 channels.
- It is divided into an A and a B side, each of which contains three Central Processors and one of each of the other elements, and can operate:
 - Either as a single logical system, with the A and B sides combined, in single image mode.
 - Or as two logical triadic systems, with the A and B sides working independently, in partitioned mode.



IBM 3090 Field Upgradeable Growth Path

Storage Hierarchy

The IBM 3090 Processor Unit has a highly efficient three-level storage hierarchy consisting of High Speed Buffer, Central Storage and optional Expanded Storage, managed by the System Control Element and Buffer Control Element.

System Control Element:

- Contains logic for the control of data storage and retrieval for the processor complex.
- Provides the communication path between Processor Storage and the rest of the processor complex.
- Performs error checking and correction.

High Speed Buffer/Buffer Control Element:

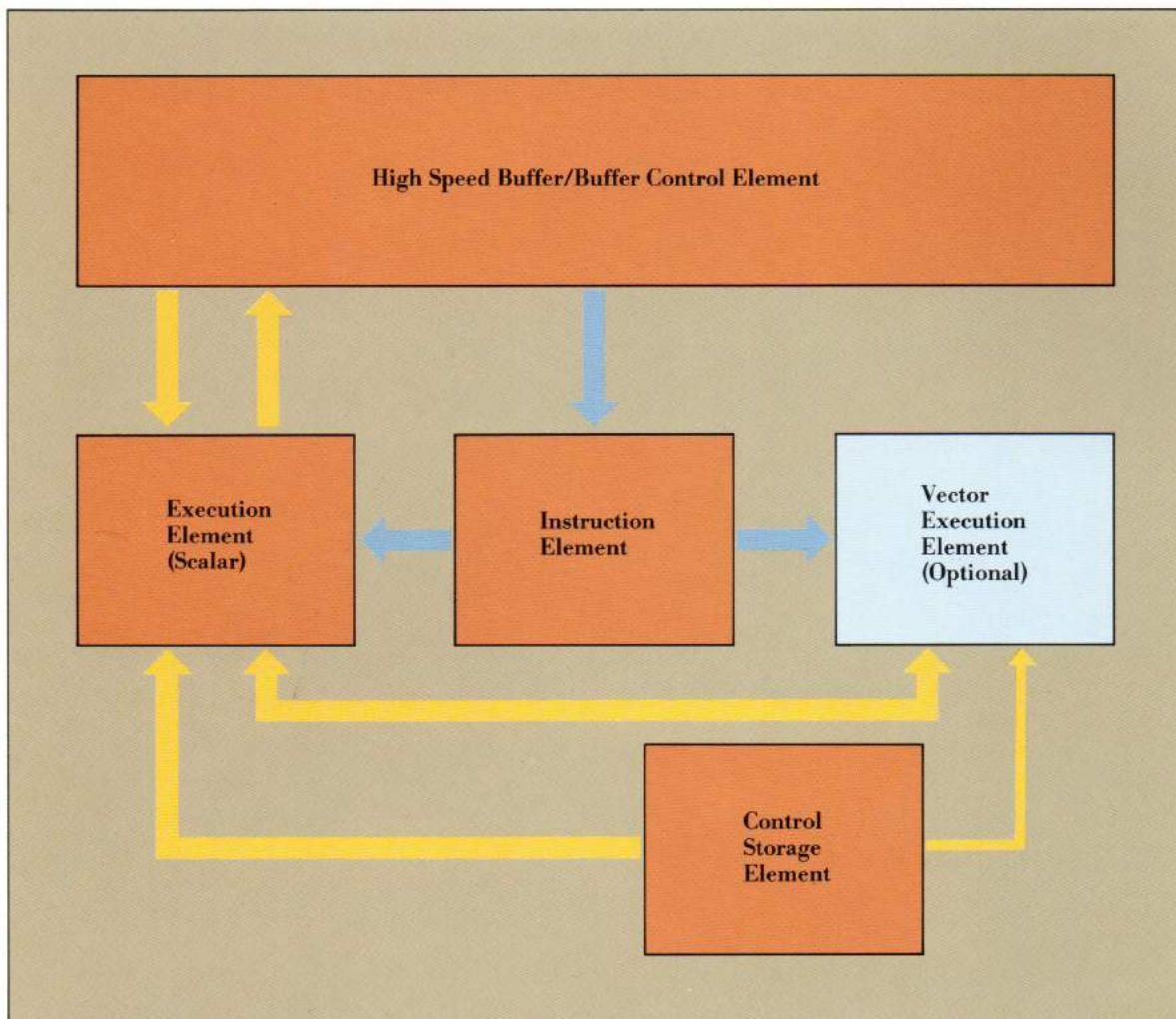
- Provides an individual storage access function for each Central Processor for active data and instructions.
- Contains a 64K-byte High Speed Buffer, Buffer Directory, Translation Look-aside Buffer (TLB) and Dynamic Address Translation (DAT) hardware.
- The High Speed Buffer is transparent to programs that are being executed.

Central Storage:

- Central Storage, using IBM-developed one megabit memory chips, is provided as follows:
 - 32 Mb for the Model 120E.
 - 32 or 64 Mb for the Models 150E and 180E.
 - 64 or 128 Mb for the Models 200E or 300E.
 - 128 or 256 Mb for the Models 400E or 600E.
- Central Storage is shared by the Central Processors in the Models 200E or 300E and can be shared or partitioned on the Models 400E or 600E.
- Central Storage, and optional Expanded Storage, are linked via Processor Storage Control to the System Control Element by a pair of 64-bit data paths.
- All single bit errors are detected and corrected. All double bit errors are detected and some are corrected.
- Dynamic frame de-allocation permits page-frames with correctable double-bit errors to be de-allocated in 4K-byte blocks under system control program control.
- Storage Protection provides Store and Fetch protection, preventing unauthorised access.

Optional Expanded Storage:

- Expanded Storage provides optional low-cost, large-capacity solid state storage using IBM-developed one megabit chips:
 - 64 or 128 Mb for the Models 120E and 150E.
 - 64, 128, 192 or 256 Mb for the Model 180E.
 - 64, 128, 192, 256 or 512 Mb for the Models 200E and 300E.
 - 128, 256, 384, 512 or 1024 Mb for the Models 400E and 600E.
- Transfer is exclusively to and from Central Storage in 4K-byte pages performed by Processor Storage Control at system control program request.
- On the Model 400E or 600E each Processor Storage Control can access the whole of Expanded Storage without transferring data through the second System Control Element.
- Expanded Storage is transparent to user programs.
- All single and double bit errors are corrected. All triple bit errors are detected and some are corrected. Four bit errors in a single block are detected.
- Expanded Storage reduces the paging and swapping load on channels and I/O devices and improves system response and performance.



IBM 3090 Central Processor Design

Central Processor

High performance processor design:

- 17.2, 17.75 or 18.5 nanosecond cycle time for the enhanced models and 18.5 nanosecond cycle time for the previously available models.
- 64K-byte High Speed Buffer for fast access to instructions and data.
- Overlapped design permits Instruction Element to decode instructions in parallel with scalar or vector instruction execution. The degree of overlap varies depending on the 3090 model.
- Up to seven instructions can be in process simultaneously in the Instruction and Execution Units of each Central Processor.
- Multi-engine design permits all of the Central Processors in the multiprocessing models to operate simultaneously.

Supports both System/370 and System/370 Extended Architecture:

- System/370 Architecture permits up to 16 Mb virtual storage per address space.
- System/370 Extended Architecture permits 2048 Mb virtual storage per address space and Bimodal Addressing for co-existence of System/370 programs.
- General purpose instruction set of 212 scalar instructions.
- 52 scalar floating point instructions.
- Short (32-bit), long (64-bit) and extended (128-bit) precision scalar floating point support.
- 16 general purpose registers (32 bits wide).
- Four 64-bit floating point registers, which can be paired for 128-bit operations.

Microcode assists for added performance:

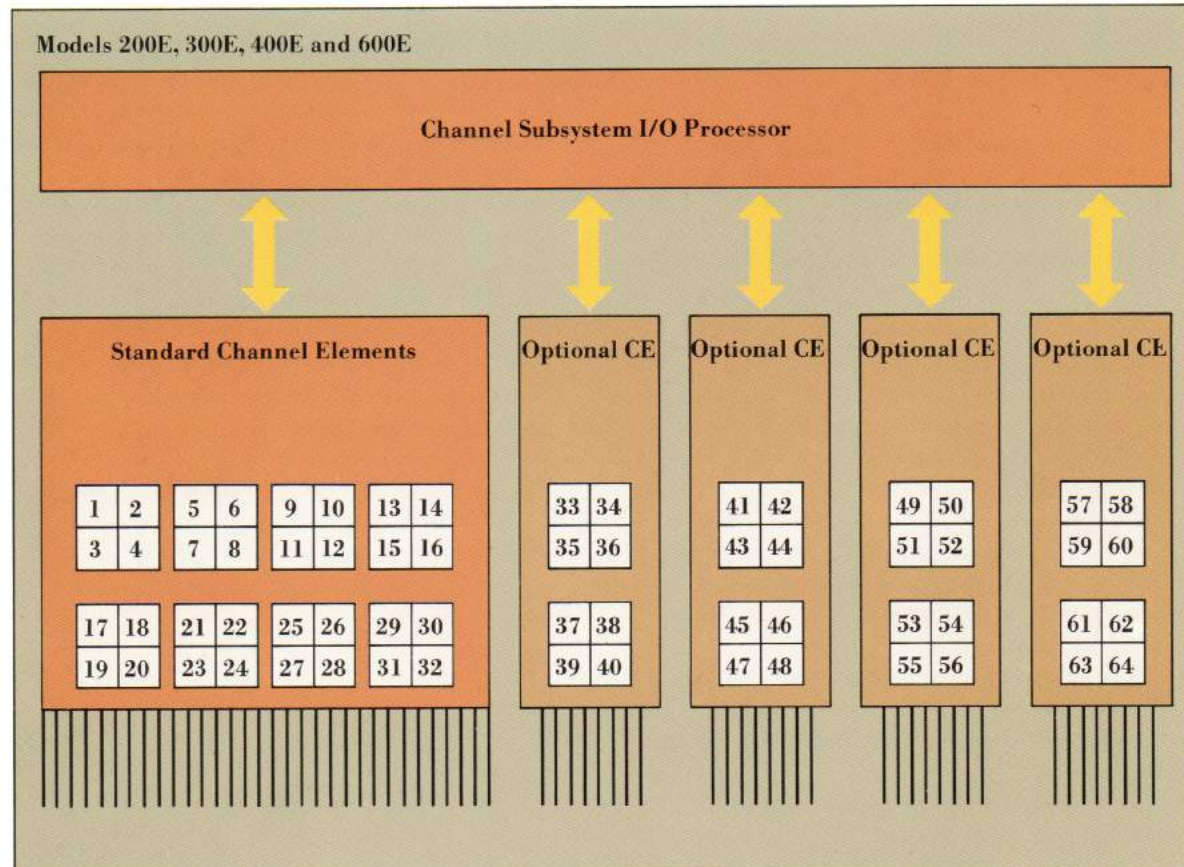
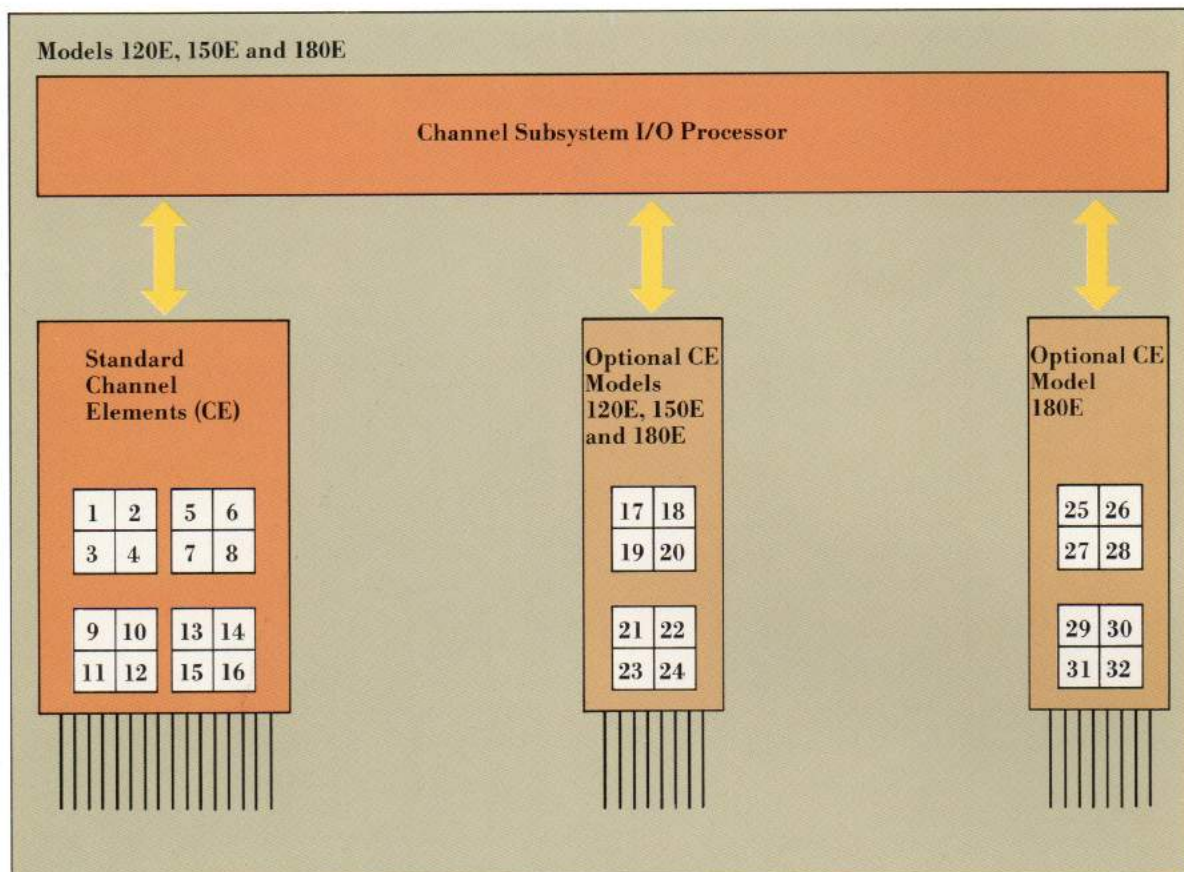
- Double capacity Control Storage Element on enhanced 3090 models stores instructions for microcoded operations and assists.
- Start Interpretative Execution (SIE) improves performance for preferred guests running under VM/XA Systems Product (SP) or VM/XA Systems Facility (SF):
 - MVS/XA performs at near native mode.
 - MVS/370 performs at 86-88% of native mode.
- Virtual Machine Assist under SIE improves performance of VM/SP and VM/SP HPO guests by approximately 20%.
- Preferred Machine Assist (PMA) enables MVS/370 guests to run at approximately 95% of native speed under the VM/SP High Performance Option.
- SORT assist improves performance of the DESORT program product.

Designed for outstanding scalar performance:

- High speed multiply implemented in hardware.
- Fast floating point add/subtract hardware.
- Special loop control circuitry.
- 64-bit wide data paths.

Optional Vector Facility:

- Provides significant performance improvements compared to scalar performance for typical vectorisable applications.
- Executes vector arithmetic and logical operations on up to 128 sets of operands with a single instruction.
- Pipelined design and compound instructions permit completion of up to two operations per cycle.
- 171 vector instructions allow arithmetic and logical operations with binary, short (32-bit) and long (64-bit) precision floating point vectors.
- 16 vector registers can each store 128 32-bit elements and can be paired for 64-bit operations.
- Three-address instruction formats minimise movement of information in registers and improve operand re-use.
- Input operands may be:
 - Vector register and vector register
 - Vector register and storage
 - Vector register and scalar register
 - Storage and scalar register
- Vector results are placed in vector registers, scalar results are placed in scalar registers.
- Addressing can be performed using fixed stride values, indirect element selection or under mask control.
- Automatic address updating handles sectioning of vectors longer than 128 elements.
- Vector Activity Register, supported by the System Measurement Facility (SMF), permits analysis of vectorisation levels achieved.
- Vector Affinity, supported by MVS/XA, VM/XA SP, VM/XA SF and VM/SP HPO, ensures that vectorised programs are run on a Central Processor which has a Vector Facility.



Channel Subsystem

- The Channel Subsystem performs I/O operations for the processor complex.
- The Models 120E, 150E, 180E, 200E and 300E have one Channel Subsystem, the Models 400E and 600E have two Channel Subsystems.
- Each Channel Subsystem contains an I/O Processor which communicates with its associated System Control Element to access Central Storage and manages up to 16 Channel Elements.
- Each Channel Element provides support for four channels. A separate microprocessor operates each channel and can support up to eight control units.
- All channels configured as block multiplexer channels can operate at 3 megabytes per second in data streaming mode and at up to 1.5 megabytes per second in interlocked mode.
- Both data streaming and non-data streaming devices may be attached to any block multiplexer channel on an intermixed basis.
- Optionally, up to four channels per Channel Control Element can be initialised to operate as byte multiplexers. This permits:
 - Up to four byte multiplexers for models 120E, 150E, 180E, 200E or 300E.
 - Up to eight byte multiplexers for models 400E or 600E.

System/370 Extended Architecture Mode Operation:

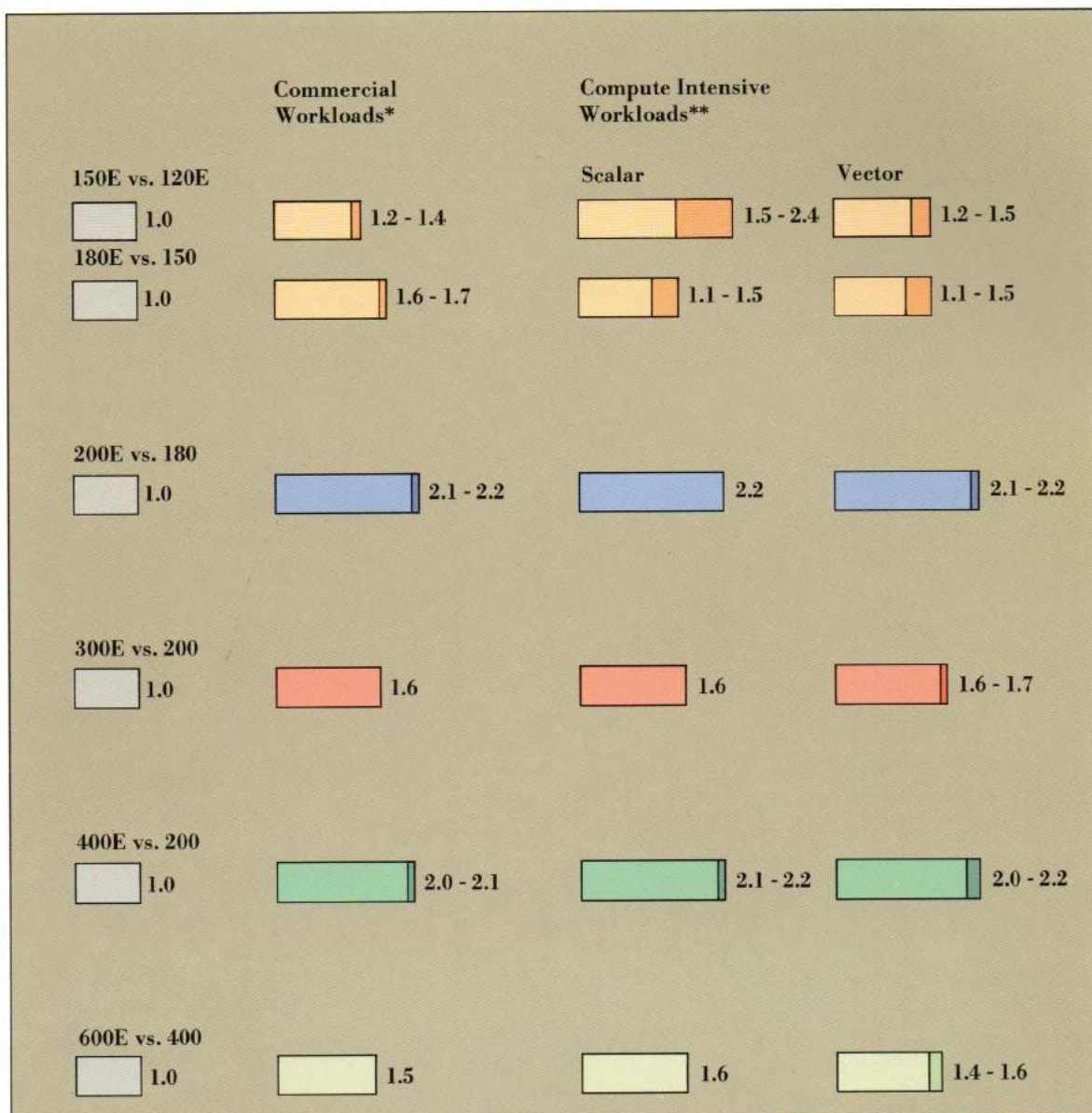
- Any processor may initiate an operation with any I/O device and process any I/O interrupt using any channel path.
- Up to four different logical paths to a single device may be used.
- In single-image mode the two Channel Subsystems of a Model 400E or 600E co-ordinate activity and appear as one dynamic Channel Subsystem to the system control program.

System/370 Mode Operation:

- Channels may be grouped into logical channel sets with one set assignable to a Central Processor.
 - MVS/370 supports a maximum of 16 channels per channel set.
 - VM/SP High Performance Option supports up to 32 channels per channel set.
- Channel Set Switching permits a change of channel set assignment in the event of a Central Processor failure, so that I/O access can be maintained.

Channel Configuration:

- The Models 120E and 150E have 16 standard channels with one optional increment, giving a maximum of 24 channels.
- The Model 180E has 16 standard channels with two optional increments, giving a maximum of 32 channels.
- The Models 200E and 300E have 32 standard channels with three optional increments, giving a maximum of 64 channels.
- The Models 400E and 600E have 64 standard channels with three optional increments, giving a maximum of 128 channels.
- The channel, control unit and device configurations are defined to the Channel Subsystem by the I/O Configuration Dataset (IOCDS) selected at system initialisation.
- The IOCDS is created by the I/O Configuration Program and stored on the IBM 3370 Direct Access Storage Devices attached to the IBM 3092 Processor Controller. Multiple IOCDSs which describe different I/O configurations may be stored.



IBM 3090 Performance Comparisons

* IERR - Internal Execution Rate Ratio
 ** ITRR - Internal Throughput Rate Ratio

Performance

Performance gains in the enhanced IBM 3090 family are achieved by means of cycle time reductions, technology improvements and design extensions.

The commercial comparisons for all models are Instruction Execution Rate Ratios (IERRs), while the comparisons for the compute intensive applications are Internal Throughput Rate Ratios (ITRRs). An ITRR is the measurement of the central processor time of a job on one system relative to the time on another system.

Additional details on 3090 scalar, vector and parallel performance for engineers, scientists and analysts may be found in the companion publication G511-0136.

Instruction Execution Enhancements:

- The 3090 offers instruction sequencing controls with an overlapped design to process instruction streams at the same time.
- Most half-word instructions are processed in a single machine cycle on the 3090 models.
- Some 3090 instructions are pre-executed to improve performance.
- On the 3090's highly overlapped central processor, up to seven instructions can be in various stages of processing at the same time.
- Decode History Table and faster loop control on the 3090 contribute to reduce the delay associated with program branches, providing overall improvement of 3090 performance.

Multiprocessor performance:

- The 3090's System Control Element utilises buses that allow transfer both to and from requestors on any given cycle.
- Most key data paths on the 3090 are parallel, which allows reading and writing to be done at the same time.

Floating Point Arithmetic Enhancements:

- Improved multiply handling provides IBM's fastest multiply time ever.
- Improved add/subtract handling provides IBM's fastest add/subtract time ever.
- Special loop-handling circuitry speeds up loop execution.

64-bit machine design:

- Data paths throughout the processor unit are 64 bits wide permitting movement of 64 bits of data or instructions per cycle.

Channels:

- Reduced Instruction Set Computing (RISC) architecture is employed by the I/O Processor in the Channel Subsystem, providing high performance, design flexibility and channel subsystem extendability.
- Each of up-to-128 channels available on the 3090 Model 600E has its own dedicated microprocessor.

System Control Program Support

The IBM 3090 Family is supported in System/370 Extended Architecture mode by MVS/XA, VM/XA Systems Product and VM/XA System Facility. In System/370 mode support is provided by MVS/370,

VM/SP High Performance Option and Airline Control Program/Transaction Processing Facility Version 2.2 Details of the support available with recent releases of MVS and VM are given below:

Function	Release	MVS/System Product		
		MVS/370	MVS/XA	
		L3	2.1.7	2.2
CPU Instructions to Enhance MVS (S/370 Extended)		•	•	•
Low Storage Protection		•	•	•
Cross-Memory Services		•	•	•
Global Resource Serialization		•	•	•
Segment Protection Within PLPA		•	•	•
3880 Buffered Paging Subsystem		•	•	•
Dynamic Channel Subsystem			•	•
31-Bit Real & Virtual Addressing			•	•
Up to 6-Way Single Image			•	•
Expanded Storage			•	•
Availability Enhancement			•	•
Vector Facility Compile		•	•	•
Vector Facility Execute			•	•

Function	Release	VM/370		VM/XA			
		VM/System Product High Performance Option (HPO)		Systems Facility		Systems Product	
		4.2	5.0	1	2	1	2
VSE and VSI Guest		•	•	•	•	•	•
MVS/370 and MVS/XA Guest plus SIE				•	•	•	•
Start Interpretive Execution (SIE) and VMA under SIE				•	•	•	•
32 Channels/Channel Set		•	•				
Dynamic Channel Subsystem (up to 128 channels)				•	•	•	•
3090 Single Image					•	•	•
64 Mb Central Storage		•	•	•	•	•	•
128 Mb Central Storage				•	•	•	•
256 Mb Central Storage					•	•	•
Expanded Storage-Paging Support		•	•		•	•	•
Expanded Storage-Guest Support				•	•	•	•
Vector Facility-Compile		•	•	•	•	•	•
Vector Facility-Execute		•	•		•	•	•
Full CMS Support		•	•			•	•
Spool File Limit Relief			•			•	•
Inter-System Facilities		•	•				
31-Bit Addressing				•	•	•	•
RACF Support		•	•			•	•
SNA Support							•
Bimodal CMS					2.2	•	•
Performance Monitoring Facility						•	•
Programmable Operator Support						•	•

Physical Characteristics

		Power cons. 400 Hz 50/60 Hz	Heat Output To Water To Air	Total	Floor Space	Including Service Clearance	Weight
		KVA	KBTU/HR		SQ MTRS SQ FT	SQ MTRS SQ FT	KG LB
120E	Min	25.3 4.4	44.4 28.7	73.1	7.4 79.9	41 443	5215 11500
	Max	33.9 4.4	55.0 37.2	92.2	8.6 92.2	46 490	5942 13100
150E	Min	26.0 4.4	44.4 31.1	75.5	7.4 79.9	41 443	5305 11700
	Max	35.0 4.4	55.3 39.9	95.2	8.6 92.2	46 490	6032 13300
180E	Min	26.5 4.4	42.7 35.5	78.2	7.4 79.9	41 443	5305 11700
	Max	40.7 4.4	61.8 48.5	110.3	8.6 92.2	46 490	6032 13300
200E	Min	36.5 4.4	63.5 41.0	104.5	7.4 79.9	41 443	5920 13050
	Max	53.8 4.4	92.9 60.1	153.0	9.3 99.3	48 515	6795 14980
300E	Min	44.3 4.4	80.6 44.0	124.6	8.6 92.2	46 490	6645 14650
	Max	63.8 4.4	116.1 63.5	179.6	9.3 99.3	48 515	7269 16026
400E	Min	71.5 8.4	127.0 76.4	203.4	14.3 153.8	68 727	11045 24350
	Max	106.1 8.4	185.8 114.6	300.4	17.3 185.9	80 864	12796 28210
600E	Min	87.2 8.4	161.2 82.6	243.8	16.0 171.7	75 815	12497 27550
	Max	126.2 8.4	232.2 121.4	353.6	17.3 185.9	80 864	13745 30302

Figures for power consumption, heat output, space requirements, and weight include IBM 3097 power and coolant distribution unit, 3092 processor controller and 3090 processor unit as minimum and maximum (includes channels, central storage, expanded storage, and vector facility).

The IBM Installation - Manual Physical Planning, GC22-7074, should be used for detailed planning.

Publications

- | | | | |
|-----------|---|-----------|---|
| S229-3299 | IBM Problem Analysis and Remote Support Reference Guide | GC22-7072 | IBM General Information Manual: Installation Manual |
| GA22-6974 | IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturer Information | | Physical Planning |
| GA22-7000 | IBM System/370 Principles of Operation | GC22-7074 | IBM System/370 3090 Processor Complex Installation Manual |
| GA22-7001 | IBM System/370 System Summary Processors | | Physical Planning |
| GA22-7002 | IBM System/370 Input/Output Configurator | SC38-0038 | IBM 3090 Processor Complex I/O Configuration Program |
| SA22-7085 | IBM System/370 Extended Architecture Principles of Operation | | User's Guide and Reference |
| SA22-7095 | IBM System/370 Extended Architecture Interpretive Execution | SC38-0039 | IBM 3090 Processor Complex: Operator Messages |
| SA22-7120 | IBM 3090 Channel Characteristics and Configuration Guide | | for the Systems Console |
| SA22-7121 | IBM 3090 Functional Characteristics | SC38-0040 | IBM 3090 Processor Complex: Operator Controls |
| GA32-0039 | IBM Input/Output Device Summary | | for the Systems Console |
| GC22-7064 | IBM Input/Output Equipment Installation Manual | SC38-0041 | IBM 3090 Processor Complex: Operator Tasks |
| | Physical Planning | | for the Systems Console |
| | | GX22-7107 | IBM Physical Planning Template - 3090 Processor Complex Metric Scale |
| | | GX22-7108 | IBM Physical Planning Template - 3090 Processor Complex English Scale |

IBM Eurocoordination SA
au capital de 2.700.000 F
Siège social: Tour Pascal
22 Route de la Demi-Lune
92075 Puteaux
RCS Nanterre B 304 538 192
France

IBM World Trade Asia
Pacific Group
IBM Kamiyacho Building
3-9 Toranomon 4-chome
Minato-ku
Tokyo 105 Japan

IBM World Trade
Americas Group
Town of Mount Pleasant
Route 9 North Tarrytown
New York 10591 USA

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